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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/771,547	01/30/2001	Toshiyuki Sato	D-1059	8819

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EXAMINER	
AGGARWAL, YOGESH K	
ART UNIT	**PAPER NUMBER**
2615	

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/771,547	SATO ET AL.	
	Examiner	Art Unit	
	Yogesh K. Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5 and 7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/21/2005 has been entered.

Response to Arguments

2. Applicant's arguments filed 06/21/2005 have been fully considered but they are not persuasive.

Examiner's response:

3. Applicant argues w.r.t claims 1 and 7 that in the amended claims the converting layer is formed of a vapor-deposited polycrystalline film of CdTe or CdZnTe while in the conventional radiation detector, a polycrystalline film of CdTe or CdZnTe was not made by vapor-deposition. The Examiner respectfully disagrees. As explained in the applicant's specification in Paragraph 24, Page 10 that a polycrystalline film of CdTe, CdZnTe or the like for the converting layer 1 is formed by an MOCVD method. MOCVD stands for metal organic chemical vapor deposition. Izumi et al. (US Patent # 6,344,370) teaches that a polycrystalline film made of CdTe, CdZnTe may be deposited by a MOCVD method (metal organic chemical vapor deposition, See col. 9 lines 35-45, col. 10 lines 61-64). Therefore Izumi teaches a converting layer formed of a vapor-deposited polycrystalline film of CdTe or CdZnTe.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Izumi et al. (US Patent # 6,344,370).

[Claim 1]

Applicant's admitted prior art teaches a radiation detector comprising an active matrix board (Paragraphs 1-11, figure 3, element 10) including gate lines (4) and data lines (5) arranged in a two-dimensional lattice form, a plurality of high-speed switching elements (3) provided at respective lattice points and connected to the gate lines and the data lines, each having a source electrode, pixel electrodes connected to the source electrodes of the high-speed switching elements, and charge storage capacitances (2), each being disposed between the pixel electrode and a ground electrode (Paragraph 3) and a converting layer (1) formed on the pixel electrodes to generate a pair of electron-hole by absorbing one of light and radiation (Paragraph 8).

Applicant's admitted prior art does not explicitly teach that each high-speed switching elements are formed of polycrystalline silicon thin film transistors and converting layer being formed of a polycrystalline film of CdTe or CdZnTe. However Izumi teaches a method of fabricating a two-dimensional image detector used for X-rays comprising TFTs 4 used as switching elements (col. 8 line 10, figures 1 and 2) of the active matrix substrate 1 being formed of polycrystalline-Silicon (col. 9 lines 12-17) and the semiconductor layer 19 that is a

photoconductive layer being formed of a vapor-deposited (MOCVD) polycrystalline film made of CdTe or CdZnTe (col. 9 lines 35-45, col. 10 lines 61-65, figure 2) in order to provide enhanced sensitivity to X-rays.

Therefore taking the combined teachings of Applicant's admitted prior art and Izumi, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have used poly-silicon as the material for TFTs and polycrystalline film made of CdTe or CdZnTe for the converting layer in order to provide enhanced sensitivity to X-rays as compared with a-Se, thereby enabling to obtain image data corresponding to animated drawings, that is, image data at 33 msec/frame as taught in Izumi (col. 10 line 65-col. 11 line 3).

[Claim 4]

Applicant's admitted prior art teaches wherein said active matrix board (figure 2: 10) further includes a base plate (figure 2: 11) having high heat resistance and insulating property, an insulating film (figure 2: 2b) disposed on the base plate and sandwiched by the gate lines (figure 2: 4) and data lines (figure 2: 5), an insulating protecting layer (figure 2: 12) disposed on the insulating film above the switching element, and a common electrode (figure 2: 1b) disposed on the converting layer.

[Claim 7]

Applicant's admitted prior art teaches a radiation detector comprising an active matrix board (Paragraphs 1-11, figure 3, element 10) including gate lines (4) and data lines (5) arranged in a two-dimensional lattice form, a plurality of high-speed switching elements (3) provided at respective lattice points and connected to the gate lines and the data lines, each having a source electrode, pixel electrodes connected to the source electrodes of the high-speed switching

elements, and charge storage capacitances (2), each being disposed between the pixel electrode and a ground electrode (Paragraph 3) and a converting layer (1) formed on the pixel electrodes to generate a pair of electron-hole by absorbing one of light and radiation (Paragraph 8).

Applicant's admitted prior art does not explicitly teach that each high-speed switching elements are formed of polycrystalline silicon thin film transistors with a heat resistant temperature more than 300C and converting layer being formed of a polycrystalline film of CdTe or CdZnTe having a film-forming temperature higher than 300C. However Izumi teaches a method of fabricating a two-dimensional image detector used for X-rays comprising TFTs 4 used as switching elements (col. 8 line 10, figures 1 and 2) of the active matrix substrate 1 being formed of polycrystalline-Silicon (col. 9 lines 12-17) and the semiconductor layer 19 that is a photoconductive layer being provided being formed of a vapor-deposited (MOCVD) polycrystalline film made of CdTe or CdZnTe with a film formation temperature of not lower than 400 C (col. 9 lines 35-45, col. 10 lines 61-65, figure 2). The Examiner notes that Poly-silicon has a melting point of 1400 degrees C which is well above 300 degree C. Therefore poly-silicon inherently has a heat resistant temperature of more than 300 degree C. Therefore Izumi inherently disclose a switching element having a temperature above 300 degree C. Furthermore, Izumi teaches the combination of poly-Si (TFTs) and Polycrystalline film made of CdTe or CdZnTe wherein the film formation temperature is not lower than 400 C (col. 10 lines 61-65) which means that the heat resistant temperature for poly-silicon must be more than 300 C so that the polycrystalline film made of CdTe or CdZnTe can be easily deposited on the active matrix board 1.

Therefore taking the combined teachings of Applicant's admitted prior art and Izumi, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have used poly-silicon as the material for TFTs with a heat resistant temperature of more than 300 C and polycrystalline film made of CdTe or CdZnTe for the converting layer with a film formation temperature of not lower than 400 C in order to provide enhanced sensitivity to X-rays as compared with a-Se, thereby enabling to obtain image data corresponding to animated drawings, that is, image data at 33 msec/frame as taught in Izumi (col. 10 line 65-col. 11 line 3).

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art in view of Izumi et al. (US Patent # 6,344,370) in further view of Yamazaki (US PG-PUB # 2002/0163035).

[Claim 5]

Applicant's admitted prior art teaches a radiation detector comprising gate driving circuit (figure 3: 6) to be connected to the gate lines (figure 3: 4), a signal driving circuit (figure 3: 7) to be connected to the data lines (figure 3: 5). Applicant's admitted prior art fails to teach a signal process circuit formed on the active matrix board for connecting the gate lines and data lines to the gate driving circuit and the signal driving circuit. However Yamazaki teaches a signal processing circuits (figure 8: 702 and 703) formed on the active matrix board substrate (figure 8: 100) and connected to the pixel section 701 through gate wiring 704 and source wiring 158 (Paragraph 135). Therefore taking the combined teachings of Applicant's admitted prior art in view of Izumi it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have a signal process circuit formed on the active matrix board for

connecting the gate lines and data lines to the gate driving circuit and the signal driving circuit as taught in Yamazaki in order to improve the operation performance and the reliability of a semiconductor device by properly using the TFT structures on the same substrate as taught in Yamazaki (Paragraph 19).

Conclusion

7. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
August 22, 2005

DAVID L. OMETZ
SUPERVISORY PATENT
EXAMINER